

L1 Global Muon Trigger Update

URL of this presentation:

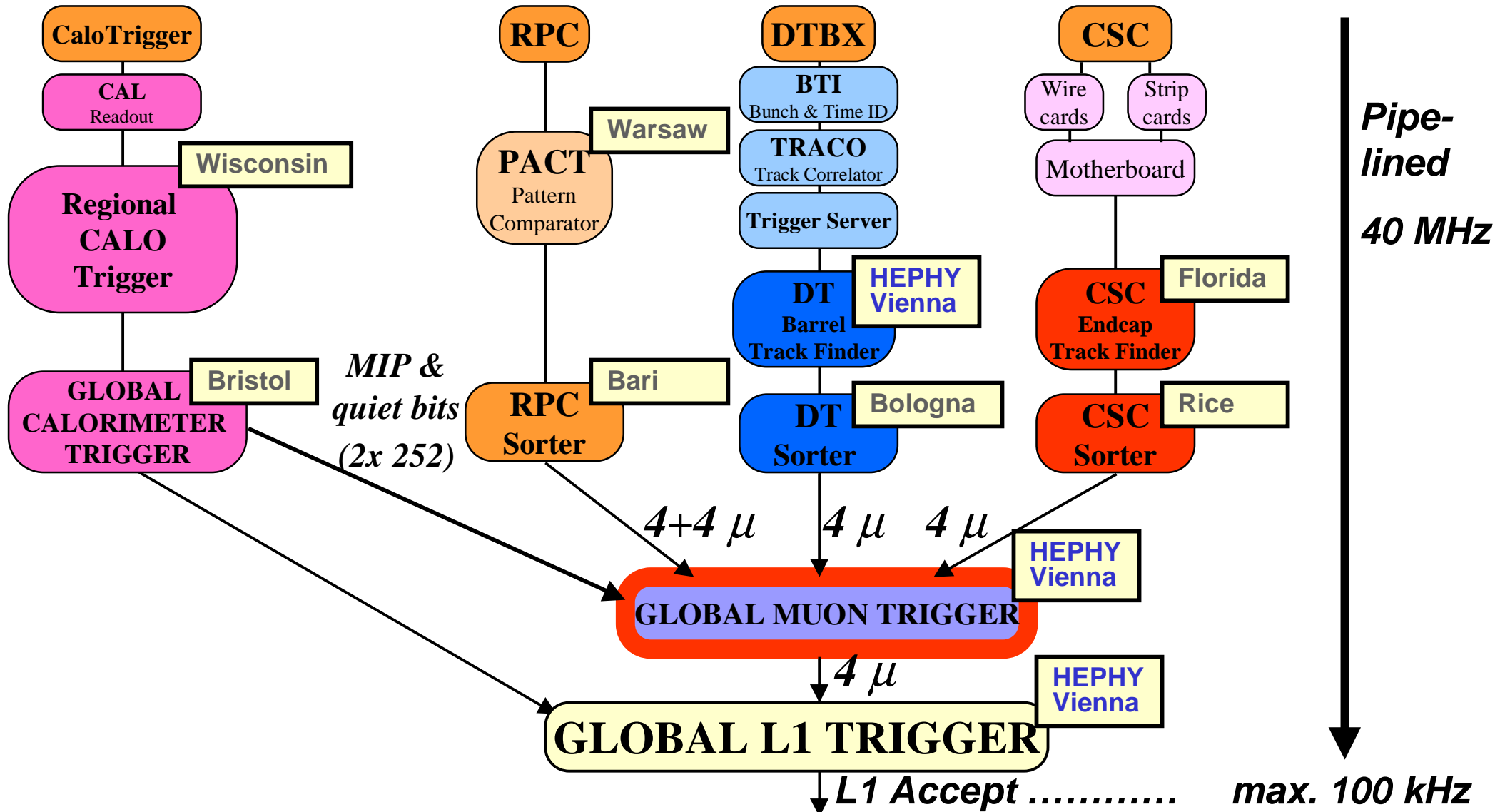
<http://wwwhephy.oeaw.ac.at/p3w/cms/trigger/globalMuonTrigger/trans/GMT-IntReview24Sep2001.pdf>

Hannes Sakulin, CERN / EP
presented by Claudia Wulz, HEPHY Vienna

Annual Review of the CMS Trigger,
CMS Week, CERN
24th September, 2001



CMS Level-1 Trigger





Tasks of the GMT



- Receive Muon Candidates from DT, CSC and RPC Triggers
- Find the best 4 muons in the detector
 - ⇒ Make use of the complementarity of the muon triggers (DT/RPC barrel, CSC/RPC endcap)
 - increase efficiency
 - reduce ghosts
 - reduce trigger rate by improving p_T assignment
- Add MIP and Quiet bits from the calorimeter trigger
- Forward best 4 muons to the Global L1 Trigger



Principle of the GMT

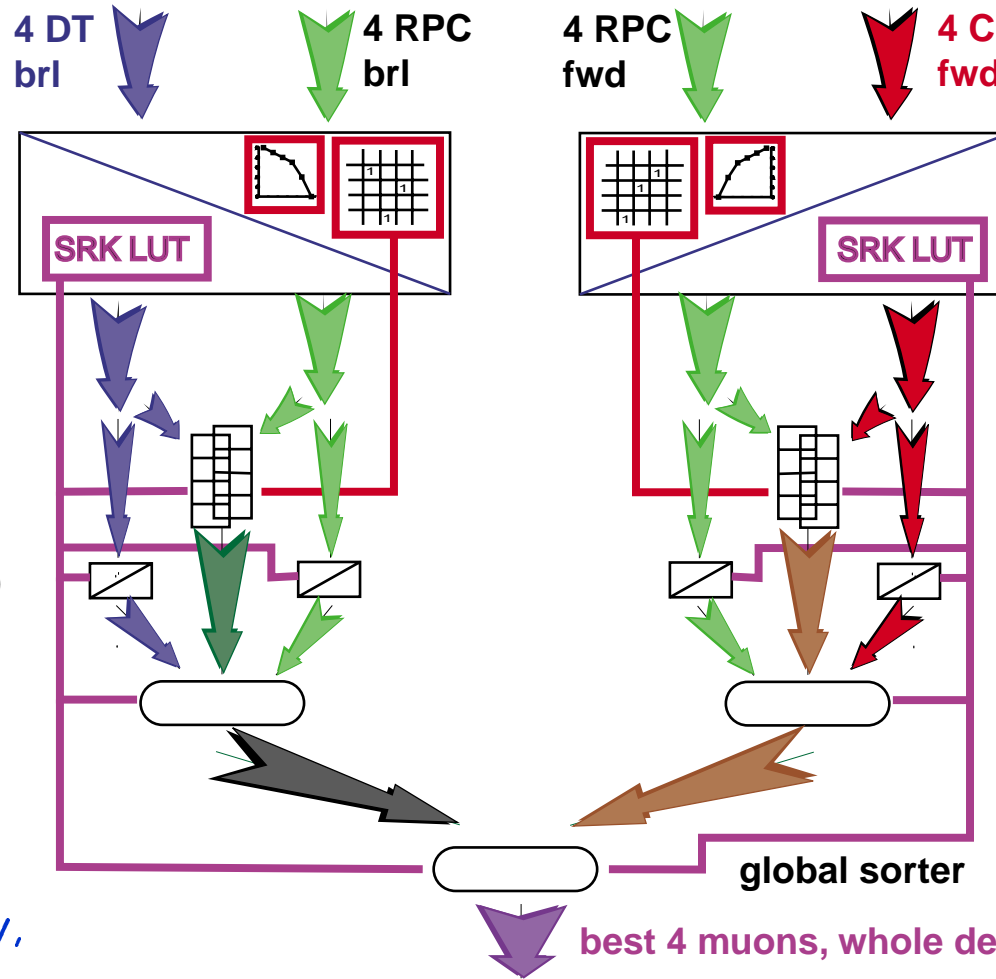


Inputs:

8 bit ϕ , 6 bit η , 5 bit p_T ,
1 bit charge, 3 bit quality

Further Inputs:

MIP and Quiet Bits of
252 calorimeter regions



selector (ghost suppression)

barrel sorter

Output:

8 bit ϕ , 6 bit η , 5 bit p_T ,
1 bit charge, 3 bit quality,
1 bit MIP, 1 bit Isolation

matching, finding pairs
calculating single rank

merging parameters

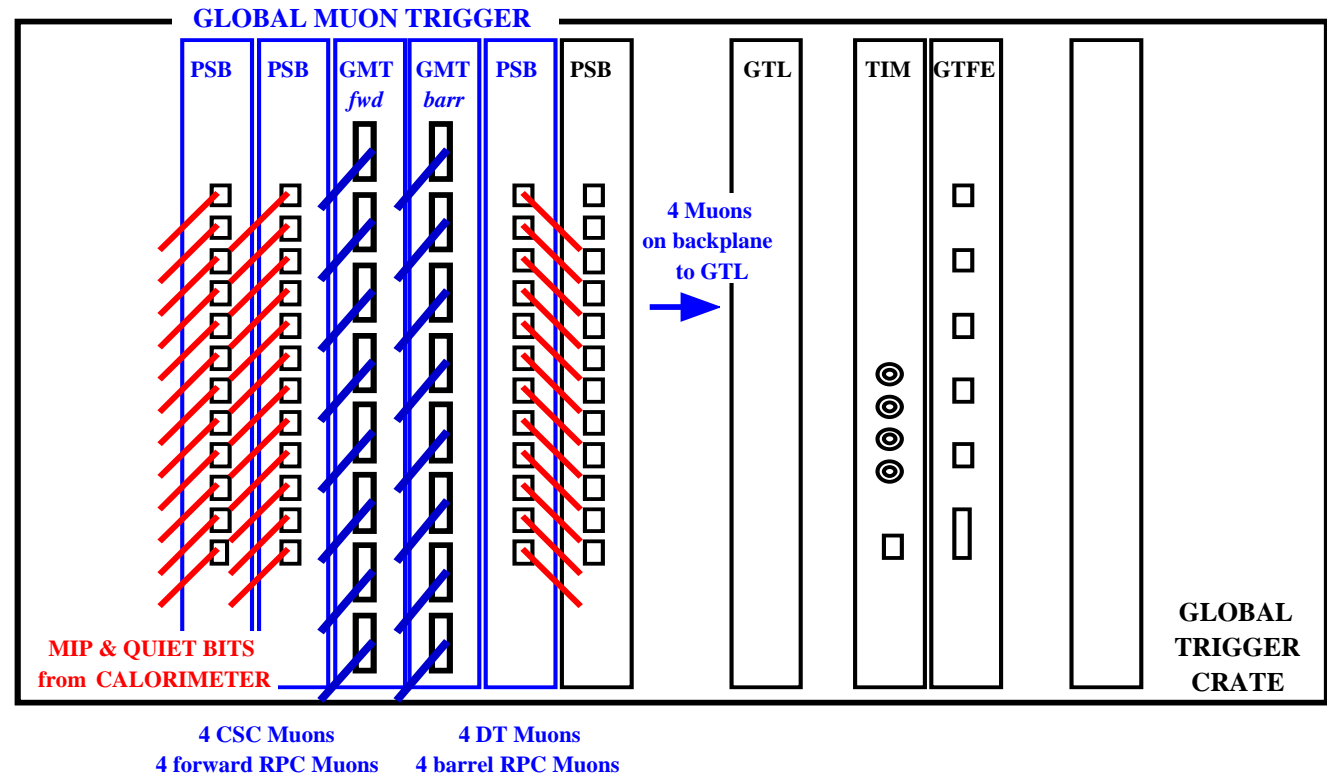
selector (ghost suppression)

forward sorter

Responsibles:

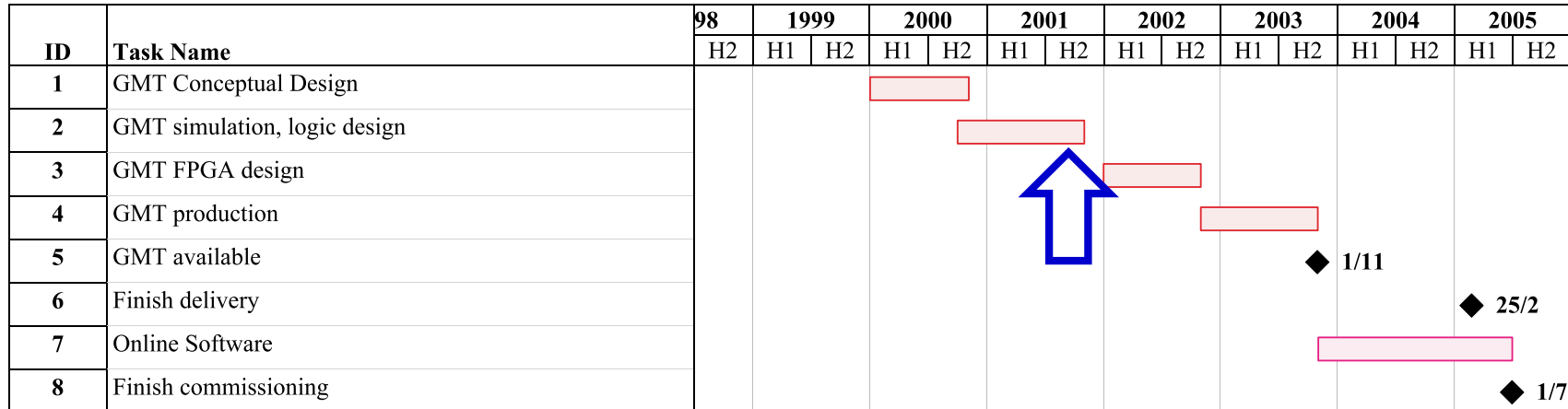
A. Taurok,
C.-E. Wulz,
H. Sakulin

- GMT is located in the Global Trigger Crate
 - ⇒ 3 PSB boards to receive calorimeter information
 - ⇒ 2 GMT Logic Boards (barrel / forward)





GMT Hardware schedule



➤ Milestones / Plans:

- ⇒ 2001 Logic design, ORCA + VHDL Simulation
- **Dec 2001** Logic design finished
- ⇒ 2002 VHDL Simulation, Design of FPGA chips
- **Dec 2002** FPGA design finished
- ⇒ 2003 Production of VME 9U Boards
- ⇒ 2004/05 Integration tests, production of spare boards



Progress towards GMT Milestones



- **Dec 2001:** **Logic design finished**
 - ✓ Progress in detailed logic design
 - Chip Models selected (mostly Virtex II), Interconnections defined
 - Design compacted (external RAMs moved into big FPGAs)
 - ✓ Improvement of functionality
 - DT/CSC cancel-out unit (improved performance in barrel/endcap overlap region)
 - ✓ in parallel:
 - ORCA Simulation extended and improved
 - Continuous studies to optimize GMT design parameters and performance
 - **CMS 2001/003** published: H. Sakulin, M. Fierro, “Studies of the Global Muon Trigger Performance”
- ⇒ Detailed GMT design document in preparation
- ⇒ VHDL behavioral level simulation has started
- **Dec 2002:** **FPGA design finished**
 - ✓ FPGA models have been selected
 - ⇒ Synthesis tools are being evaluated



Simulation: Muon 2001 production



➤ Monte Carlo production (Pythia 6.152, CMSIM 121)

- ⇒ new normalization (now Pythia default)
- ⇒ lower p_T -cut (p-cut) in forward region (now $p > 3.5$ GeV/c, was $p_T > 1.5$ GeV/c)
- ⇒ increased η -range up to in CMSIM (now 5.5, was 2.5)
- ⇒ muons in pile-up vetoed
- ⇒ LHC luminosity $L = 2 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1}$

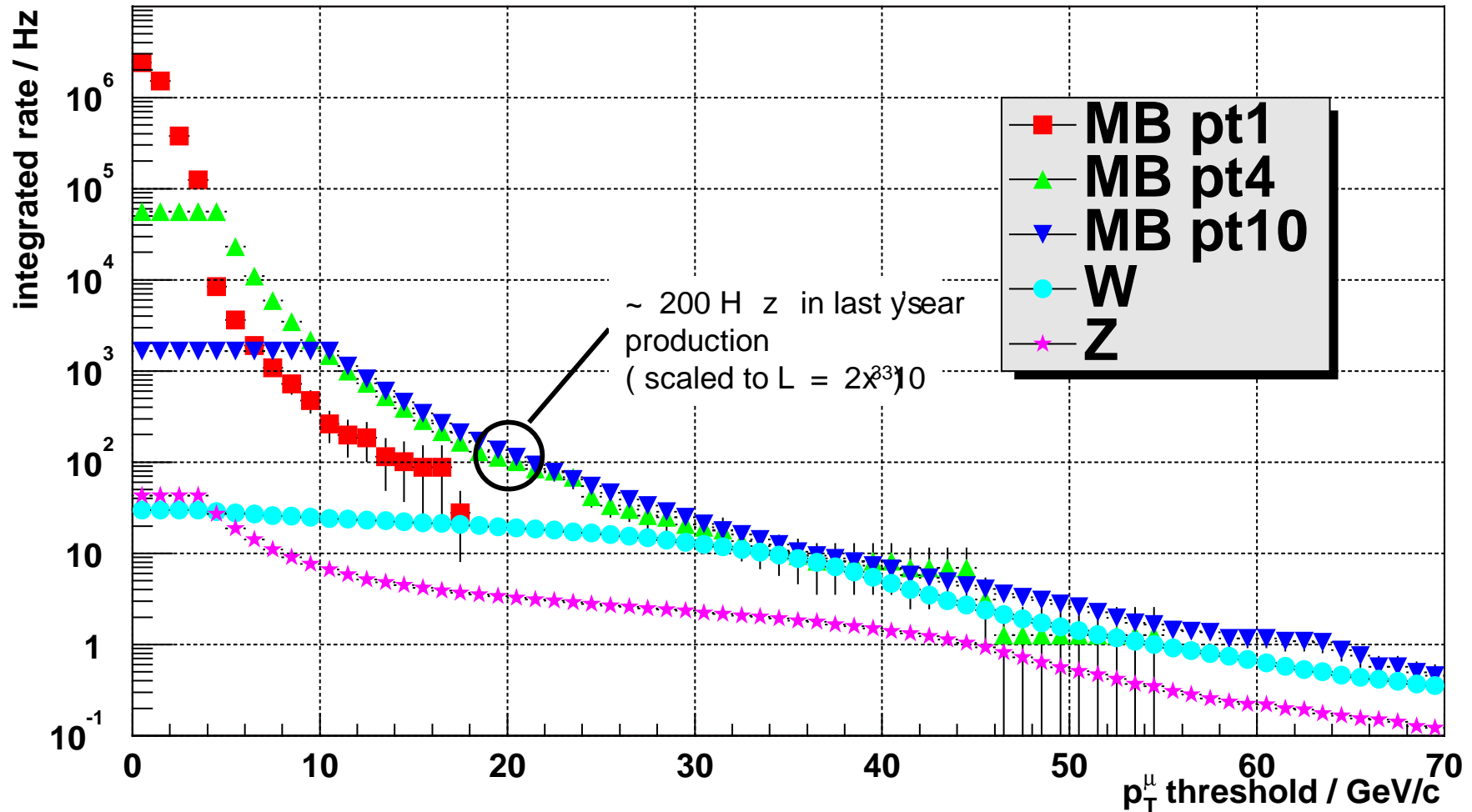
Sample	$L_{\text{int}} / \text{nb}^{-1}$	Events in luminosity
mu_MB1mu_pt1	0.0173	162k
mu_MB1mu_pt4	0.2052	54k
mu_MB1mu_pt10	2.81	41k
W_1mu	2856.	43k
Z_1mu	2336.	50k
mu_MB2mu	0.0989	11k

background samples – 2001 muon production

➤ L1 Trigger simulation (ORCA 5.1.2)

- ⇒ new CSC Trigger primitives
- ⇒ updated CSC Trigger
- ⇒ **updated Global Muon Trigger**
 - **MIP/ISO bit assignment implemented**
 - **new DT/CSC cancel-out unit**
 - **matching windows and charge assignment improved**
- ⇒ RPC: without noise and neutral background simulation

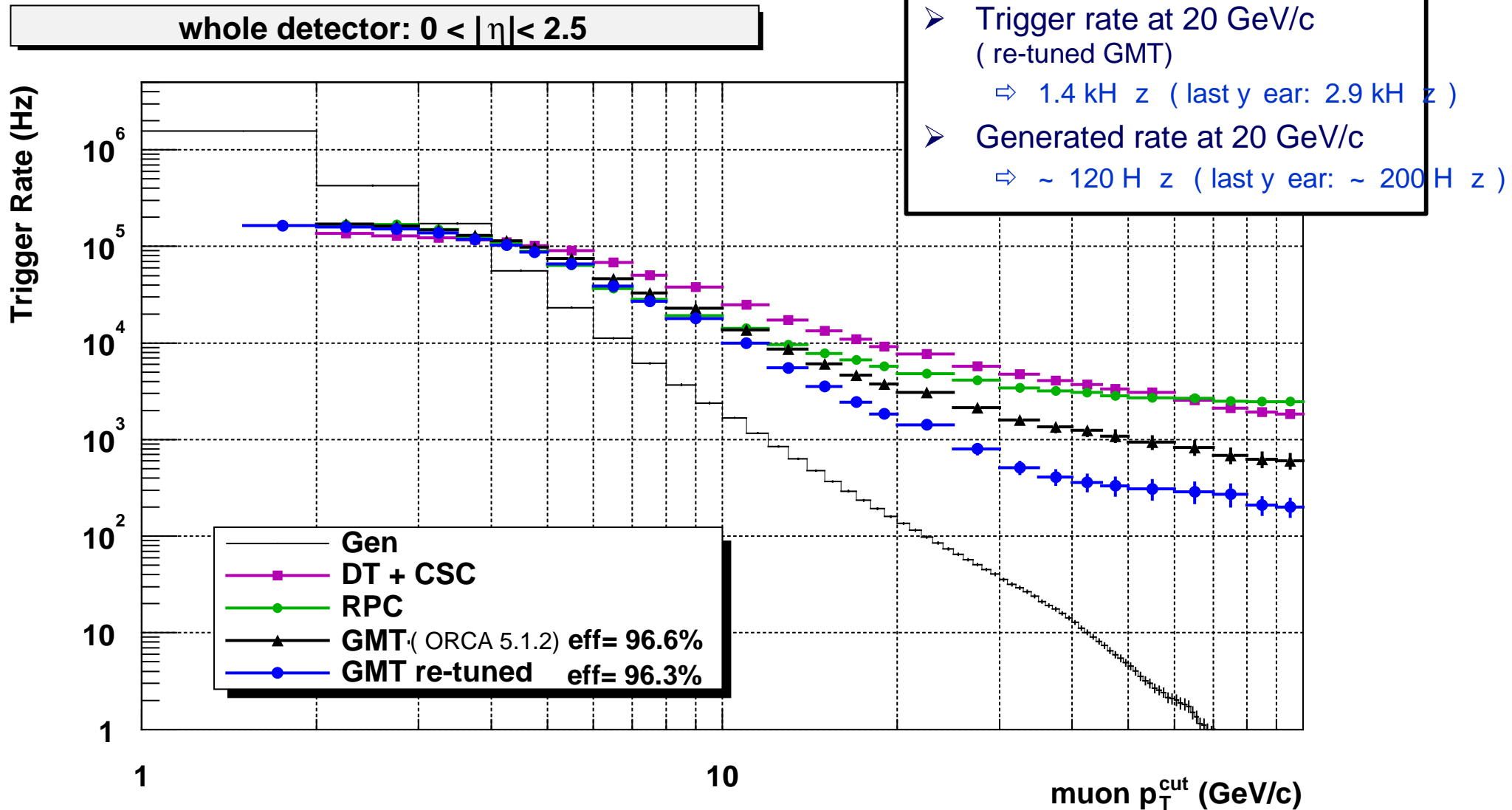
generated rates



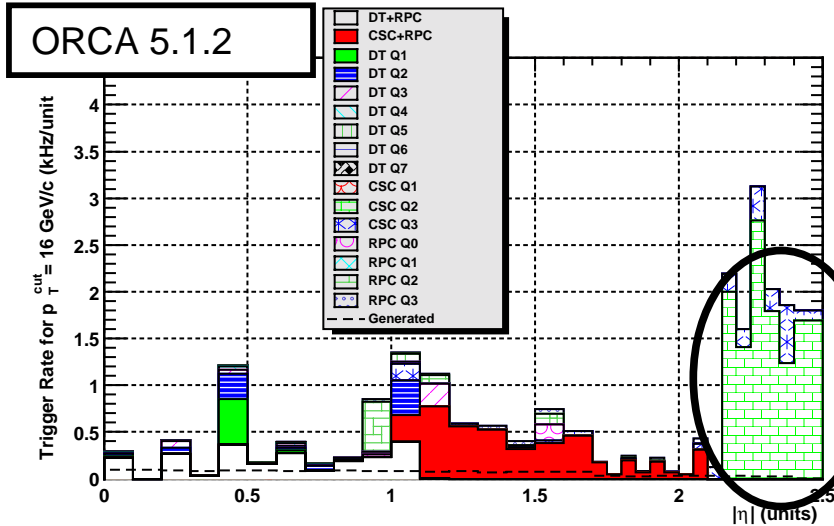


L1 single muon trigger rates

samples: pt1, pt4, pt10, W, Z, GMT re-tuned



GMT single muon trigger rates ($p_T > 16$ GeV/c)

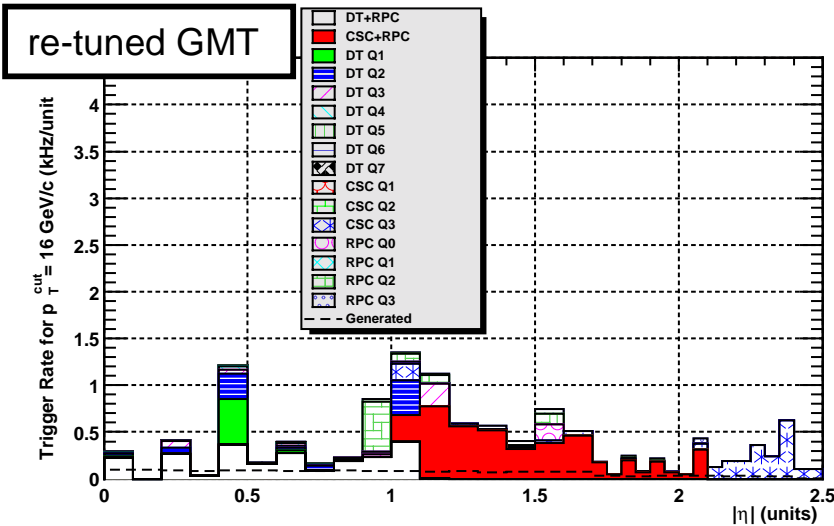


➤ GMT optimized as in ORCA 5.1.2

⇒ rate at 20 GeV/c: **3.1 kHz**

⇒ L 1 efficiency^(*): **96.6 %**

Rate from unconfirmed 2-station CSC tracks



➤ re-tuned GMT selection:

⇒ Only three-station CSC tracks used without RPC confirmation

⇒ rate at 20 GeV/c: **1.4 kHz**

⇒ L 1 efficiency^(*): **96.3 %**

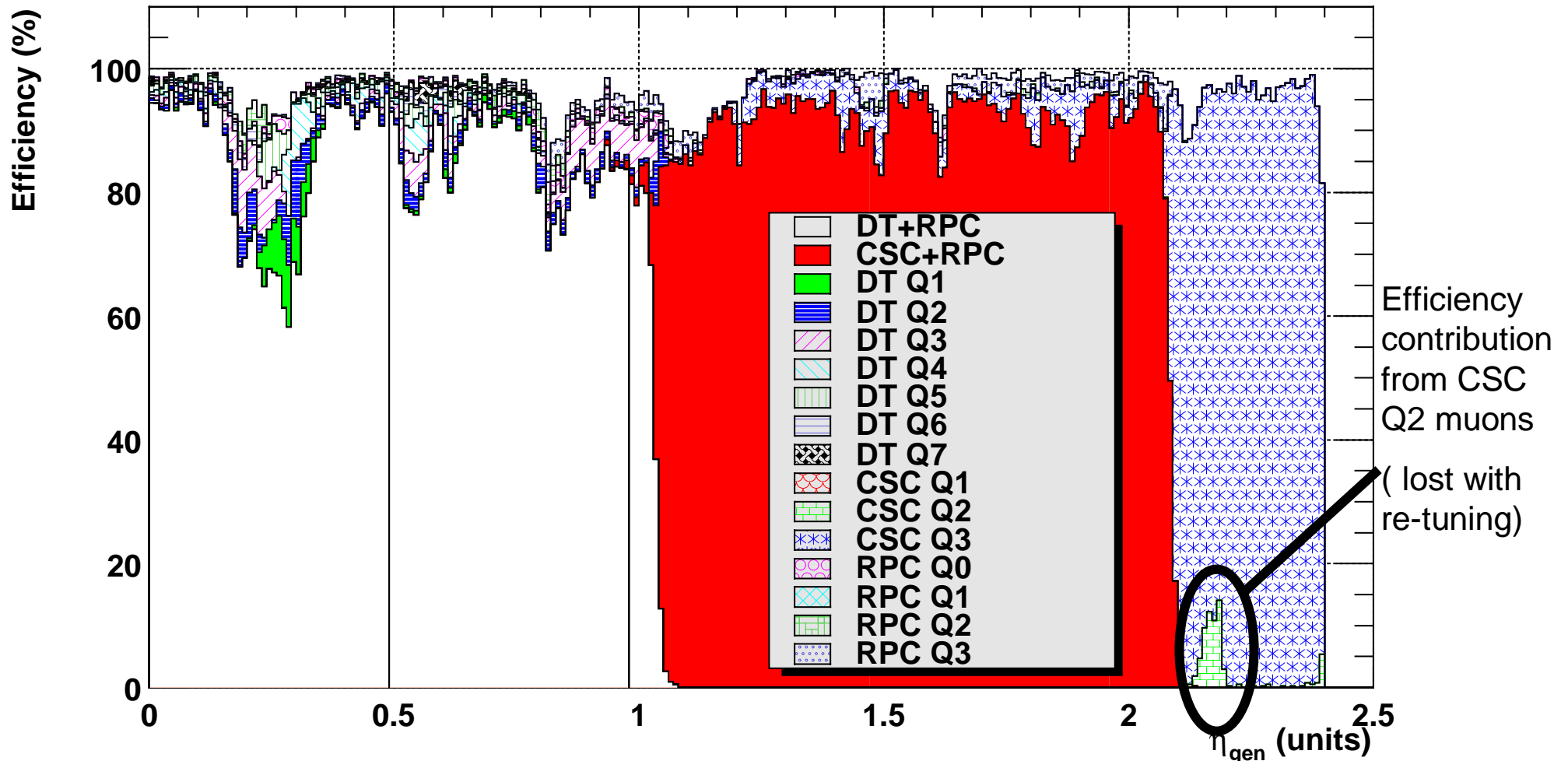
$\eta \longrightarrow$

(*)efficiency to find muon of any p_T in flat p_T sample

L1 Efficiency with re-tuned GMT

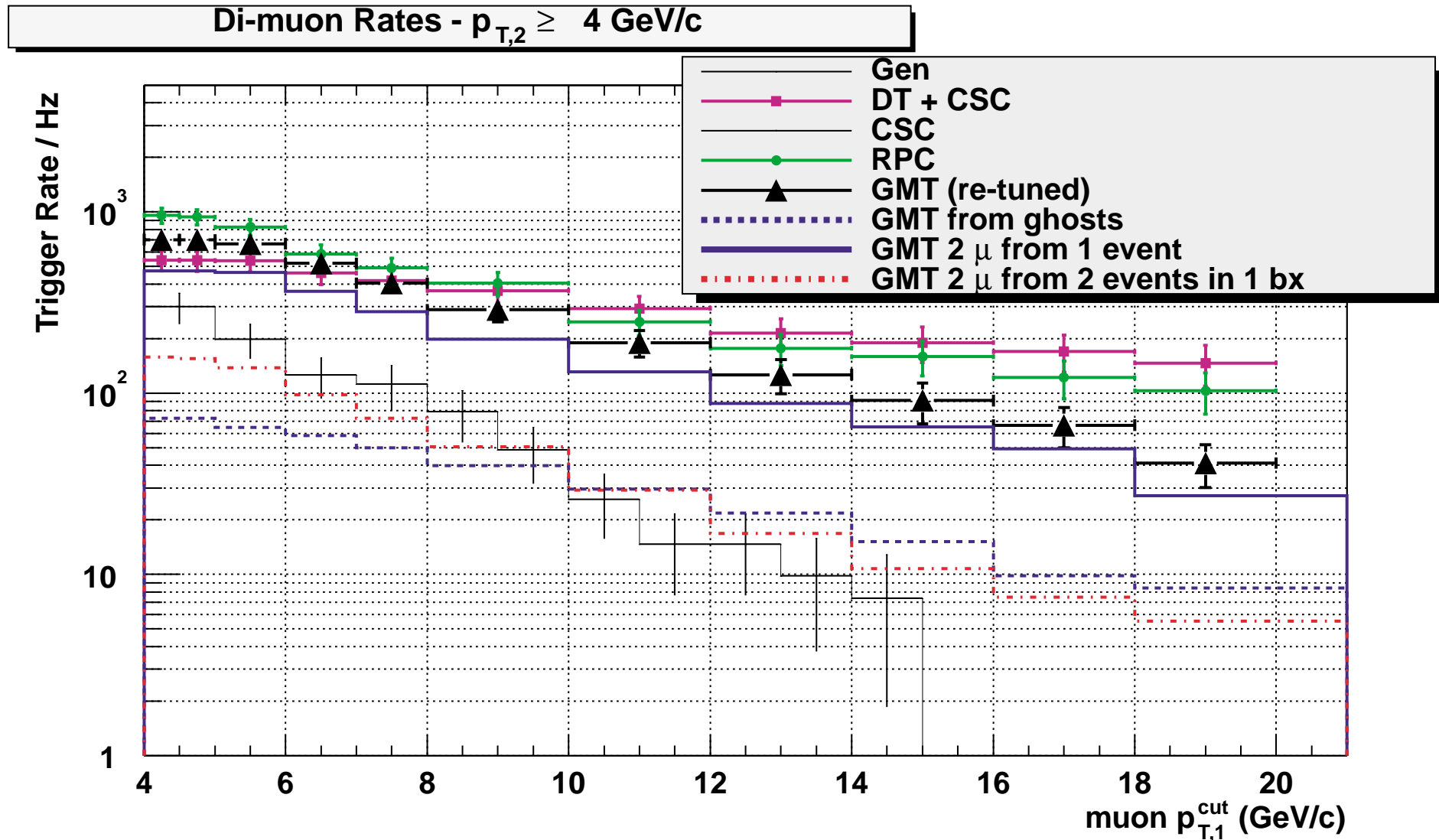
GMT efficiency to find any muon in a flat μ sample as in ORCA 5.1.2 w/o RPC noise

ORCA 5.1.2 re-tuned **eff= 96.6%**
eff= 96.3 %



L1 di-muon trigger rates, $p_{T,2} \geq 4 \text{ GeV/c}$

samples: pt1, pt4, pt10, 2mu_pt1, GMT re-tuned



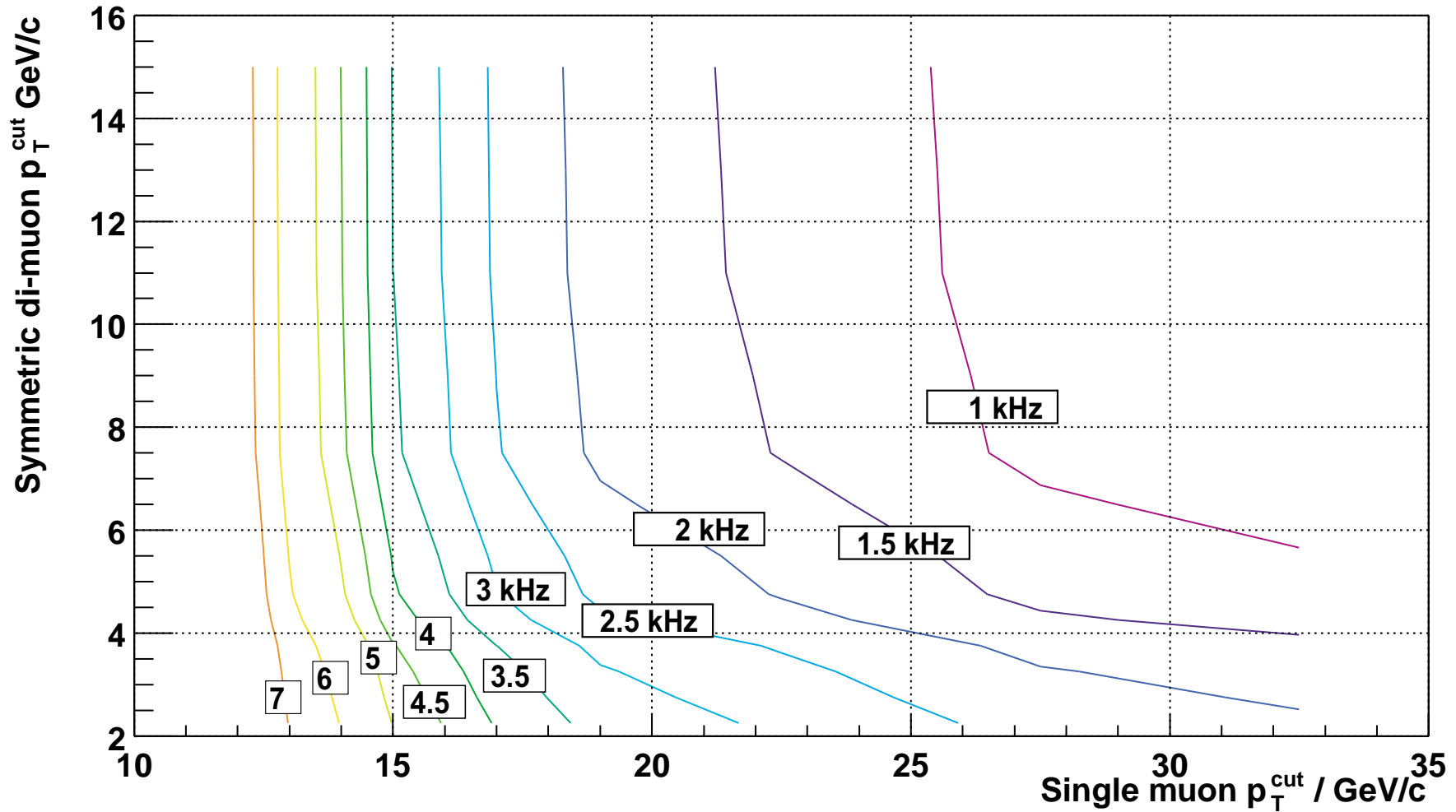


L1 single & di-muon trigger rates

symmetric di-muon cut, re-tuned GMT



L1 single and di-muon trigger rates





Conclusion



- Progress in hardware design as planned
 - ⇒ FPGA Chips selected
 - ⇒ design compacted
 - ⇒ new solution with 1 logic board
 - ⇒ VH DL simulations have started

- New simulation results with 2001 muon production
 - ⇒ p_T -cut was lower than in last year's production
 - ⇒ improved CSC trigger & GMT can cope with higher background rate
 - ⇒ trigger rates with improved trigger are lower despite higher background (even after taking into account the changed sample normalization)